A Smart CMOS Imager with On-chip High-speed Windowed Centroiding Capability

Chao Sun, Guang Yang, Christopher Wrigley, Orly Yadid-Pecht, and Bedabrata Pain*

Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109
Phone: (818)-354-5021, Fax: (818)-393-0045, E-mail: chao.sun@jpl.nasa.gov

Low-power, high-speed, accurate computation of centroid from a pre-defined window in the image plane is important for a number of space-based and commercial applications. These include object tracking in robotic systems [1], autonomous navigation, image compression [2], and document copyright protection [3], as well as space guidance and navigation systems [4], and deep-space optical communication systems that require accurate and stable beam pointing for high speed data transfer [5].

Off-focal-plane digital processors yield accurate centroid values, but only at the cost of increased latency, power and size. On or near focal plane centroid computation using current mode circuits [6], and neuro-MOS circuits [7] have been implemented. However, neither approaches are integrated with high performance image sensors, nor are they entirely compatible with one. In this paper, we present a CMOS active pixel sensor (APS) with an integrated centroid-computation circuit that allows accurate X and Y centroid computation from a user-selectable window of interest. Such an imager offers real-time centroid computation while dissipating low-power and realizing a miniature tracking system.

passive capacitor bank

The architecture of the windowed-centroiding APS (WINCAPS) is shown in Figure 1. It consists of a 2-D imager array, a switching network, inner-product (IP) computation circuits, and an analog divider. On-chip 2-D centroid computation is carried out by first computing the relevant inner-products (weighted sums) for a given row. Upon of completion of all row-wise IPs, these values are used to generate the final X and Y IP as shown in figure 1. A single divider circuit is then used to generate the X and Y centroids.

The X- and the Y-centroids computed by the on-focal-plane circuits are given by:

$$\overline{X_{nxn}} = \frac{2\cdot(n+1)}{[n(n-1)+2]}\cdot\frac{\sum_{i=1}^{n}\sum_{j=1}^{n} x_{j-1}v_{ij}}{\sum_{i=1}^{n}\sum_{j=1}^{n} v_{ij}} \qquad \overline{Y_{nxn}} = \frac{2}{(n-1)}\cdot\frac{\sum_{i=1}^{n} y_{i-1}\sum_{j=1}^{n} v_{ij}}{\sum_{i=1}^{n}\sum_{j=1}^{n} v_{ij}} \tag{1}$$

where x_i, *and* y_j =1, 2, 3, ...n-1, respectively, v_{ij} is the voltage of each pixel. Apart from a scaling pre-factor, both computations yield the correct value of the respective centroids.

Figure 2 shows the schematic of the circuit used for IP computation for the X and Y-centroid block. Only capacitors and switches are used to perform the computation [8], with different sized capacitors representing different weights. The capacitors in the column-averaging bank are used for sampling one row of pixel values. The capacitors are linearly scaled in the X-centroid block, while they are the same in the Y-centroid block. However, the sampling capacitor sizes are linearly scaled for each successive row by successively enabling EN1, EN2 ... EN(n-1) clocks. Averaging over the columns, and sharing the result with one of the capacitors in the row-averaging bank is carried out by pulsing AVC and the appropriate DUMP(i) simultaneously. This allows equal and minimal attenuation for all row signals.

The capacitors in the row averaging bank are linearly scaled for the Y-centroid block, while they are equal for the other. A switching network consisting of a Nx9 (N is the imager format) switching array connects 9 consecutive columns of the imager array into the computation circuit. This allows centroid computation

* *Electrical and Computer Engineering Department, Ben-Gurion University, P.O.B. 653, Beer-Sheva 84105, Israel*

for blocks of size 3x3 to 9x9. Thus, the computation is performed in parallel with the imager readout, leading to a high computation speed and minimal computational overhead.

Figure 3 shows the circuit schematic of the divider circuit, and figure 4 shows the chip picture of the prototype imager of 128x128 format. Computation circuits take up only a small 1.7 mm x 0.9 mm area, irrespective of the imager format. The imager was fabricated using HP 0.5-μm CMOS technology with a 12-μm pixel pitch, and has two ports: one for centroid output and the other for imager output. The imager performance summarized in table 1 shows excellent imager performance. Use of passive components and only one op-amp (for the divider circuit) enable low power (< 2 mW) operation.

In order measure the centroiding accuracy, image centroid was computed separately by acquiring the raw data from the imager port. The computed centroid was then compared against the value obtained from the centroid port, and relative error (in pixels) was computed. The measurements were repeated for different window sizes, centroid values, mean signal strengths, and from different regions of the imager. It was found that a typical centroid error of 0.02 pixel was achieved over most of the array, the worst case error being around 0.07 pixel for the smallest sized (3x3) window, as shown in figure 5. Figure 5 shows the smallest and the largest centroid error measured from the array. The error dependence on the window size was not large, although in general, the error was found to be lower for larger sized windows.

High update rates were obtained without compromising centroiding accuracy. Update rates varied from 20 to 50 kHz for window sizes scaling from 9x9 to 3x3. Irrespective of window sizes, total noise added by all three centroid computation circuits is insignificant compared to the imager output r.m.s. noise of 225 μV (~ 9 e^-). This is achieved by increasing capacitor sizes, with minimum being 2 pF. Large capacitance size also helps minimize capacitance matching errors. Residual error in the circuit is governed by matching errors and switch feedthrough. This can be seen from the fact that the centroiding inaccuracy tends to increase for mean signals less than 100 mV, as shown in figure 6. Error also increases for larger mean signals (~ 800 mV), due to non-linearities and signal saturation. As shown in table 1, saturation signal is 850 mV.

In conclusion, we have demonstrated a smart CMOS APS with integrated windowed centroid computation circuits that outputs centroid values with better than 0.05 pixel accuracy under most lighting conditions, while maintaining high update rates (20-50 kHz) that make the chip attractive for use in real-time image-based control systems.

The research described in this paper was performed at the Jet Propulsion Laboratory-Center for Integrated Space Microsystems, California Institute of Technology, under contract with the National Aeronautics and Space Administration.

REFERENCES:

1. Ishi, Y. Nakabo, and M. Ishikawa, "Target tracking algorithm for 1 ms visual feedback system using massively parallel processing," in Proc. IEEE Int. Conf. On Robotics and Automation, 1996.
2. K. Karadimitiou and J.M. Tyler, "The centroid method for compressing sets of similar images," Pattern Recognition Letters, Vol. 19, pp. 585-593, 1998.
3. S. Low, N.F. Maxemchuk, and A. M. Lapone, "Document identification for copyright protection using centroid detection," IEEE Trans. on Communications, vol. 46 (3), pp. 372-383, 1998.
4. C. C. Liebe, E. W. Dennison, B. Hancock, R.C. Stirbl, and B. Pain, "Active pixel sensor (APS) based star tracker," Proc. IEEE Aerospace Conference, pp. 256-261, 1998.
5. J. W. Alexander, S. Lee, C.-C. Chen, "Pointing and Tracking concepts for deep-space missions," in Free-Space Laser Communication Technologies XI, Proc. of SPIE vol. 3615, pp. 230-249, 1999.
6. S. Deweerth, "Analog VLSI circuits for stimulus localization and centroid computation," International Journal of Computer Vision, vol. 8 (2), pp. 191-202, 1992.

7. N.M. Yu, T. Shibata, and T. Ohmi, "A real-time center-of-mass tracker circuit implemented by neuron MOS technology," IEEE Trans. on Circuits and Systems, vol. 45 (4), pp. 495-503, 1998.
8. S.E. Kemeny, R. Panicacci, B. Pain, L. Matthies, and E.R. Fossum, "Multiresolution image sensor," IEEE Trans. on Circuits and Systems for Video Technology, vol. 7 (4), pp. 575-583, 1997.

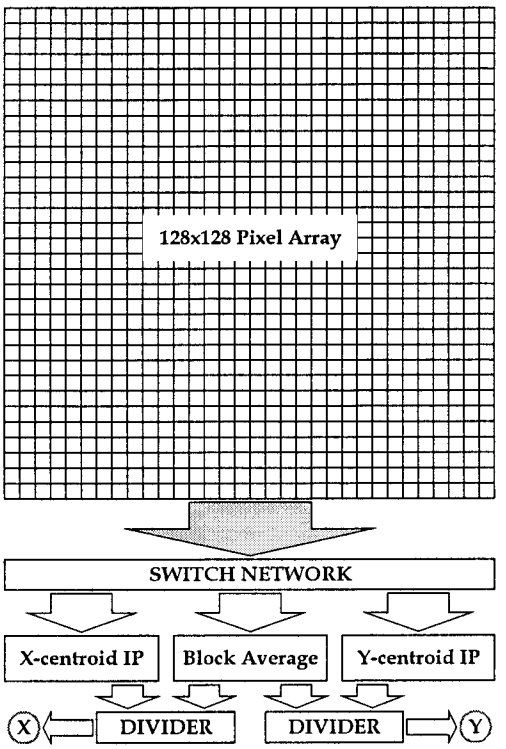

Figure 1. *Block diagram of CMOS APS with on chip windowed centroiding capability.*

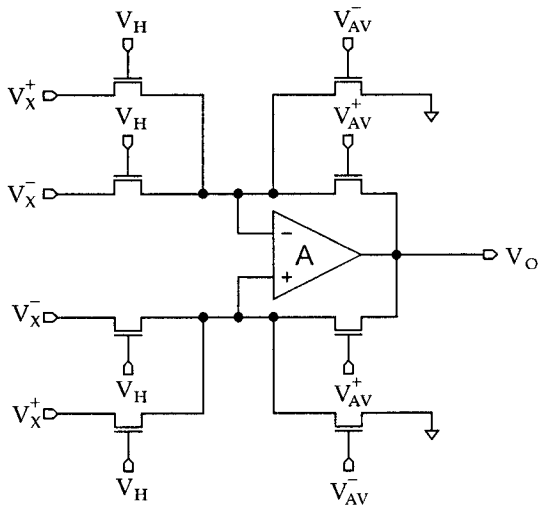

Figure 3. *Schematic of the divider circuit.*

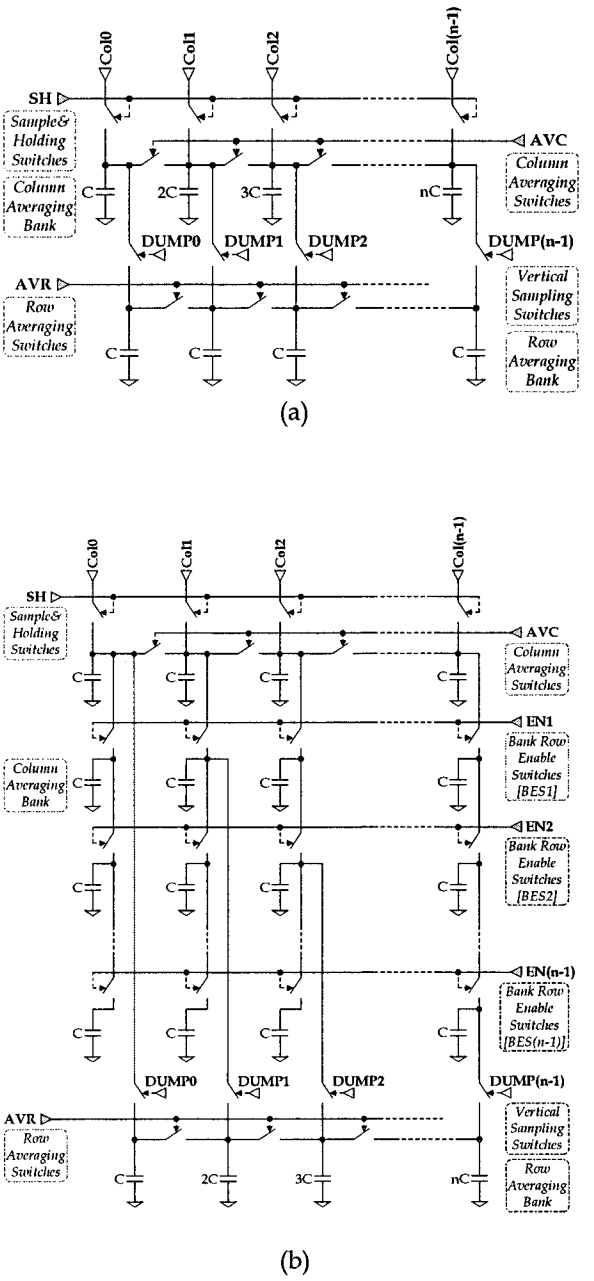

Figure 2. *Schematic of centroid IR circuit (a) X-centroid, and (b) Y-centroid.*

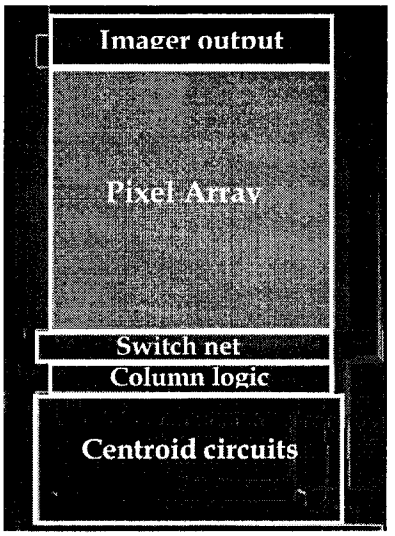

Figure 4. *Chip Photograph of the 128x128 CMOS APS centroid chip.*

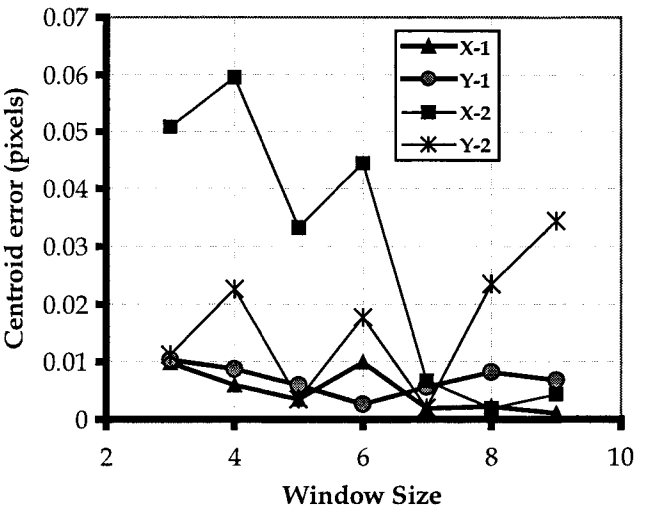

Figure 5. *Measured centroid error vs Window Size (for different window locations).*

Table 1. *Summary of the centroid APS chip characteristic.*

Characteristics	Value
Format	128x128
Pixel Size	12 μm
Technology	HP 0.5μm
Power Supply	3.3 V
Saturation Level	850mV
Conversion Gain	25μV/e-
Read Noise	9 e-
Dark Current	78mV/sec
Power	3 mW

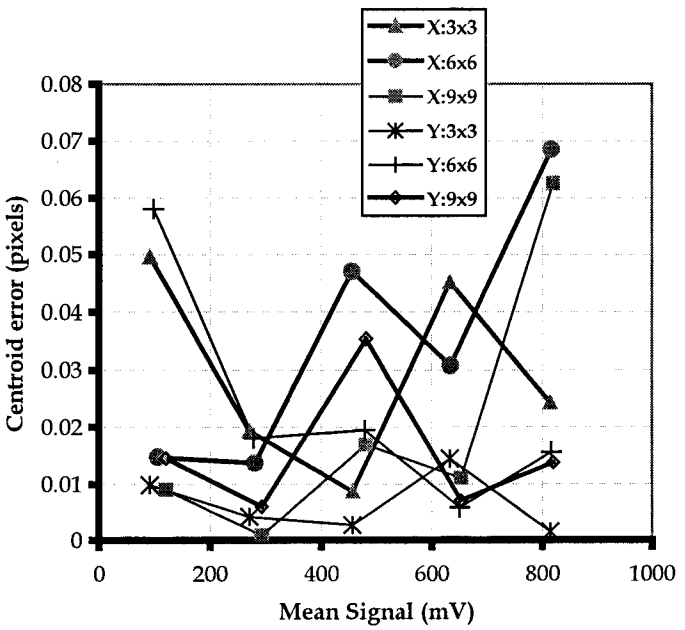

Figure 6. *Centroid error as a function of average signal strength. (for selected window sizes)*